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Denoising of Electroencephalogram Signals Using Digital Signal Processor

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Abstract: Electroencephalogram (EEG) signal is very complex and random in nature. Due to its lower amplitude, it is contaminated with many artifacts such as power line noise, baseline noise, Electromyogram (EMG), Electrocardiogram (ECG), etc. These artifacts contaminated the property of the original signal. These signals cannot be properly analyzed due to the presence of the artifacts; therefore, it is necessary to remove the artifacts before processing the raw signal. Powerline interference is the most common artifact that corrupts the EEG record of every patient. This paper emphasizes on to removing Powerline artifact with FIR notch filter and implementing it on the real time Digital Signal Processor (DSP) board of Texas TMS320C6711

Keywords: EEG signal, FIR filter, Digital Signal Processor

1. INTRODUCTION

The electroencephalogram (EEG) was first measured in humans by Hans Berger in 1929 [1]. There are many other methods for recording the brain activity which provides accurate precision and resolution of spatial localization of brain activity but EEG is widely used in clinical research and work due to its lower costs, relative ease of use and excellent time resolution [2]. Most waves ranges from 0.5-500 Hz, but most clinical EEGs have been performed with upper ranges 20-40 Hz. The familiar classification of EEG is based on frequency. i.e.; Alpha waves (8-13 Hz), Beta waves (Greater than 13 Hz), Theta waves (3.5-7.5 Hz), Delta waves (3 Hz or less).

EEG signal is contaminated by artifacts during recording and transmission process. The different artifacts are electrooculographic (EOG) artifacts, Electrocardiograph artifacts (ECG), electromyographic (EMG) artifacts, baseline noise, and power line noise. Powerline noise is a 50 Hz noise signal that appears in EEG record during the recording of EEG signal by the acquisition system. Removal of powerline noise is necessary before any further signal processing for accurate analysis of EEG signal.

Many researchers have proposed different methods using different processors and software because DSP methods are programmable, reliable, high precision and maintainable, easy to design and obtain a linear phase so that the filters don't distort the original signal [3]. A digital filter when compared to analog filter, can avoid temperature drift, noise, voltage balance. It also meets the requirement of phase and amplitude response [4]. TMS320C6711 is a floating- point digital signal processor which is based on Very Long Instruction Word (VLIW) architecture, performs intensive computations. This paper fully take advantages of MATLAB, Code Composer Studio and TMS320C6711 for designing FIR filter to remove powerline frequency of 50 Hz.

2. METHODOLOGY

DSP system comprises of Analog-to-Digital (ADC), processor and Digital-to-Analog (DAC). An input filter is used for antialiasing which eliminates the erroneous signal and an output filter to reconstruct the processed output.

The output was finally displayed in CRO as shown in last section of fig 1.

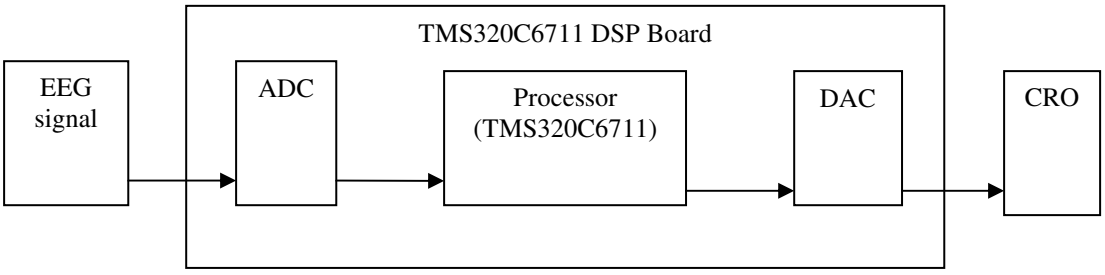


Fig1: Block diagram of methodology

For this purpose, AD535 (16-bit Codec) is provided in TMS320C6711 DSP board. EEG signal received by ADC in real time was further processed by digital signal processor (TMS320C6711) and output was then provided through DAC.

The sampling frequency of the board fixed to 8000 samples/sec does not allow the processing of low frequency signal i.e.; EEG signal because the order of the filter was increased to a high value and thus, the sampling frequency was downsampled to 1000 samples/sec. Hence, FIR notch filter centered at 50 Hz using Kaiser Window was then applied to the incoming EEG signal at sampling frequency 1000 samples/sec. Since, the antialiasing and reconstruction filters in AD535 were fixed and cannot be bypassed or altered [5], therefore, upsampling and low pass filtering were needed to output the 1000 Hz rate samples to AD535 at 8 kHz.

2.1 Basic principle of FIR:

A digital filter can be classified in to Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) according to time-domain characteristic. The selection of FIR and IIR depend on the requirements and specifications of frequency response. In designing FIR filter, it is desirable for the filters to have approximately flat frequency response in passband. Another desired feature is linear phase with an integer slope which provides simple delay in time domain and phase distortion is reduced to minimum in frequency domain [6].

The advantage of FIR filter is its stability, linear phase (delays the input signal without changing the phase), easy realization, arbitrary amplitude – frequency characteristic and fractional arithmetic implementation [3].

Finite impulse response (FIR) filter is a non recursive system where output y(n) at any discrete values depends only on the past and the initial values of input x(n). A lack of feedback makes the impulse response finite [3, 7]. FIR filter is defined by the convolution of the input signal and the impulse response h(n)

$$y(n) = \sum_{k=0}^{N-1} h(k)\, x(n-k) \qquad (1)$$

Where h(k) for k=0,1,2. .. . . . , N-1 are the coefficients of the filter

The z- transform of the above equation yields:

$$Y(z) = h(0)X(z) + h(1)z^{-1}X(z) + h(2)z^{-2}X(z) + \cdots \ldots \ldots + h(N-1)z^{-(N-1)}X(z) \qquad (2)$$

Eq. 1 represents the convolution in time which is equal to the multiplication in frequency domain given as:

$$Y(z) = H(z)X(z) \qquad (3)$$

where $H(z) = ZT[h(n)]$

$$H(z) = \sum_{K=0}^{N-1} h(n)\, z^{-k} = h(0) + h(1)z^{-1} + h(2)z^{-2} + \ldots \ldots \ldots + h(N-1)z^{-(N-1)} \qquad (4)$$

The Eq. 4 shows that N-1 poles are located at origin. Hence, FIR filter is stable, with all its poles located in a unit circle. FIR filter is usually described a filter with " no poles" [5].

There are different methods through which the FIR filters can be implemented. In this paper, window function is used. The impulse response of ideal filters is of infinite duration. These cannot be implemented by hardware or by software. Therefore, there is a need to truncate them at both sides with respect to central. The sudden cutoff causes undesired effects. The window method reduces them. Windowing means that the infinite duration of impulse response $h_d(n)$ is multiplied with the finite duration window w(n) [4, 8]. The impulse response of the FIR filter yields:

$$h(n) = hd(n)\, w(n) \qquad (5)$$

The window function is divided in to fixed window and adjustable window. Fixed window functions are rectangular window, Hanning window, Hamming window and Blackmann window. Kaiser window is a kind of adjustable window function.

Kaiser window is the best method as it provides adjustment in between the overshoot reduction and transition bandwidth region [4, 8]. Kaiser window is defined by

$$w(n) = \frac{Io[\beta\sqrt{\left(1-\left[\frac{n-\alpha}{\alpha}\right]^2\right)}]}{Io(\beta)} \qquad (6)$$

Where α = N/2 and Io(β) is a zeroth order Bessel function generated by power series expansion

$$Io(\beta) = 1 + \sum_{k=1}^{\infty}[(x/2)k / k!] \qquad (7)$$

The parameter β controls the trade-off between the side-lobe amplitude and main-lobe amplitude. It also determines the shape of the window.

Designing of FIR filter using Code Composer Studio Version 2 and FDATOOL

The convolution Eq. (1) is used to program FIR filter in C code using Code Composer Studio version 2. The impulse response coefficients are arranged in an array h[N] so that first coefficient is placed at h(0) i.e.; beginning of an array and last coefficient h(N-1) resides at the end of the array. The delay sample array, dly[N] is organised such that the newest input sample x(n) is at the beginning of buffer and the oldest sample x(n-(N-1)) is at the end of buffer. The impulse response h[N]

is obtained by setting the parameters in FDATOOL of MATLAB [5].

At time n, x(n) is acquired through ADC and stored at the beginning of the delay sample buffer dly[N]. Filter output y(n) is computed as below:

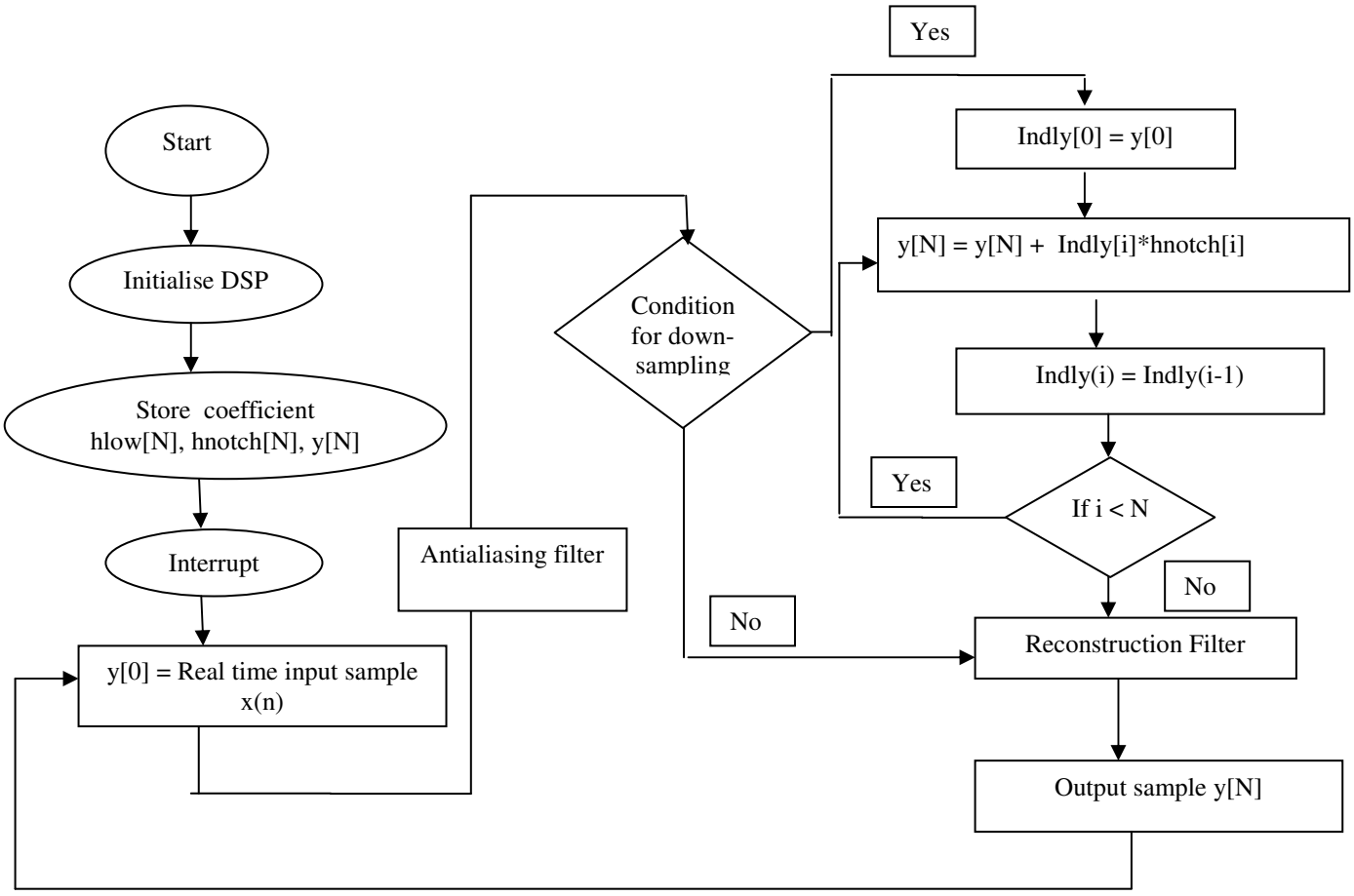
$$y(n) = h(0)x(n) + h(1)x(n-1) + \ldots\ldots\ldots + h(N-2)x(n-(N-2)) + h(N-1)x(n-(N-1)) \quad (8)$$

All the delay samples are updated to calculate y(n+1) such that x(n) stores the value of x(n-1), x(n-(N-1) stores the value of x(n-(N-2)) and so on. At time n+1, a new input sample x(n+1) is stored at the beginning of the buffer. The output y(n+1) becomes:

$$y(n+1) = h(0)x(n+1) + h(1)x(n) + \ldots\ldots\ldots + h(N-2)x(n-(N-3)) + h(N-1)x(n-(N-2)) \quad (9)$$

Again the delay buffer is updated and the output y(n+2) is calculated. This process continues for each sample period.

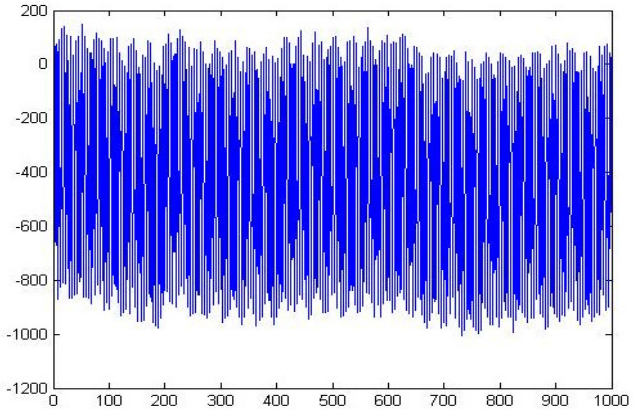
The algorithm for FIR notch filter centered at 50Hz is shown in Fig. 2



3. RESULTS AND DISCUSSIONS

The above discussed method was performed on EEG signal containing spikes of 50 Hz. The spike at 50 Hz in fig 5 clearly shows that EEG signal is contaminated with powerline noise which acted as an input to TMS32C6711 DSP board.

The final output after applying FIR notch filter centered in the range of 48-52 Hz based on the Kaiser window having order of 500 and sampling frequency 1000 samples/sec was displayed in CRO as shown in fig 6. The fig. 6 indicates that the powerline noise is reduced efficiently by removing the peak at 50 Hz.



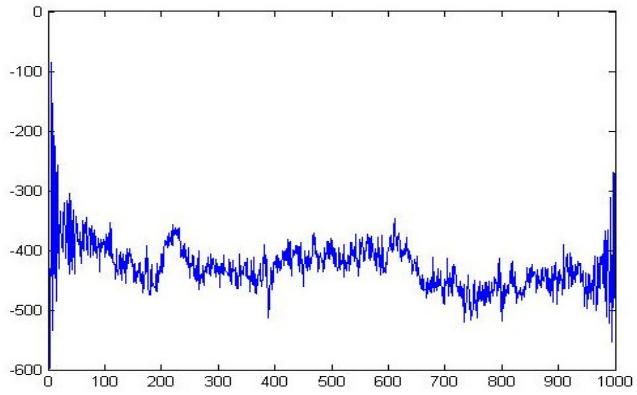
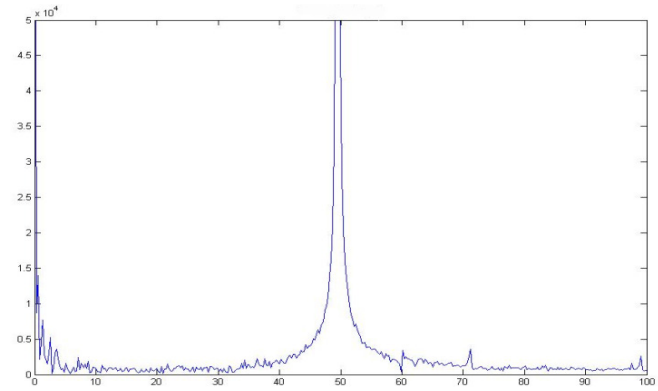


Fig 3. EEG Signal contaminated with 50Hz noise Fig 4. EEG Signal after filtration



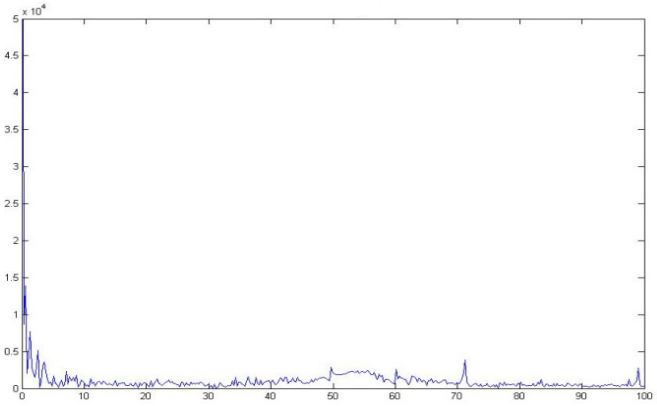


Fig 5. FFT of EEG signal contaminated with noise Fig 6. FFT of EEG signal without noise(50 Hz)

4. CONCLUSION

In this paper, EEG signal containing the spurious peaks of AC power supply was treated. This paper concludes that the powerline noise can be removed efficiently using a stand-alone system i.e.; through TMS320C6711 digital signal processor board in real time. Therefore, there is no requirement of storing the data for performing any processing on it. Moreover, many other filters can also be designed for other biological signals to remove any noise using TMS320C6711 DSP board.

REFERENCES

[1] Rohtash Dhiman, J.S. Saini, Priyanka, A.P Mittal. Artifact removal from EEG recordings – an overview. National Conference on Computational Instrumentation CSIO Chandigarh, 2010; 62-66

[2] A.GuruvaReddy , Srilatha Narava. Artifact removal from EEG Signals. International Journal of Computer Applications 2013; 77(13):16-19

[3] Aarti J. Patel, Prof. Vandana Patel. Nyquist Filter Design to Remove Power Line Interference From Bio-Electric Signals. International Journal of Engineering Trends and Technology 2012; 3(2): 81-83

[4] Chen-Long Hu. Design and Verification of FIR Filter Based on Matlab and DSP. International Conferece on Image Analysis and Signal Processing (IASP) 2012; 1- 4

[5] Rulph Chassaing. DSP Applications using C and the TMS320C6X DSK. John Wiley & Sons, INC., 2002

[6] Nirav Raghajibhai Patel. Design & Performance Comparison of FIR Low Pass Filter Using Kaiser Window & Remez Exchange Algorithm". International Journal of Emerging Trends in Electrical and Electronics 2013; 5(1): 1-6

[7] Smt.D.Swetha, Ms.K.Suneetha Krishna, Ms.A.Saritha & Ms.V.Shamily. Design of fir BSF using modified Hamming window. Journal of Information, Knowledge and Research in Electronics and Communication Engineering 2012; 2(1):311-315

[8] Alia Ahmed Eleti, Amer R. Zerek. FIR Digital Filter Design By Using Windows Method With MATLAB. International conference on Sciences and Techniques of Automatic control & computer engineering 2013; 282-287